*Attorney Docket No.: 100111257-1*

## REMARKS

Claims 1-20 remain pending in the instant application, of which claims 1, 5, 7, 13 and 18 are independent.

Claim 7 is amended without new matter.

It is believed that the above amendments and following remarks attend to all issues presented in the pending Office Action dated September 08, 2006. Where used herein, numbered subtitles reflect the numbering of issues presented in the aforementioned the Office Action.

### 4 – 5. Claim Objections

The Examiner objects to claim 7 under 37 C.F.R. 1.75 (d)(1) as reciting "responsive to comparison of a difference." . In accordance with the Examiner's objection, and suggested amendment, the term subsequent occurrences of *"responsive to comparison of a difference"* have been changed to *"responsive to detection of a difference"*. We respectfully request withdrawal of the Examiner's objection.

### 6-11. Claim Rejections – 35 U.S.C. § 103

8. Claims 1 and 4 stand rejected under 35 U.S.C. § 103(a) as being unpatentable by U.S. Patent 6,370,675 (hereinafter, "Matsumura"), in view of U.S. Patent 7,072,818 (hereinafter, "Beardslee"), and further in view of U.S. Patent 5,617,146 (hereinafter, "Duffield"), and U.S. Patent 6,115,034 (hereinafter, "Tanaka").

Respectfully, we disagree.

By way of background, the '769 Application teaches methods and systems for establishing data model consistency across one or more modules within a multiple program electronic computer aided design (E-CAD) tool. In particular, consistency of a data model is established between sub-modules of an E-CAD tool by execution of a comparison module (e.g., comparison module 111, Figure 1) that detects whether a data model under analysis has been modified since a previous analysis. A consistency database stores consistency indicators for each block in a data model. These

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consistency indicators include timestamp information of data for each block in the data model. See paragraph [0011]. As each program of the E-CAD tool runs, a comparison module (e.g., comparison module 111) is executed to compare data field values of the data model being analyzed against consistency indicators within the consistency database. See paragraph [0015]. Upon detection of a change in the data model, a warning is issued to a user to indicate the possible inaccuracy of results due to design data inconsistencies. See paragraph [0017].

On the other hand, Matsumura discloses a method for utilizing event data, derived from a dump file created by a logic simulation of a device, to produce a test pattern for use in an LSI tester. See Matsumura col. 4, lines 30-33. Matsumura then uses a comparator to compare the timing relationship between the output data of the device under test and the dump file. See Matsumura Abstract. Matsumura makes no disclosure regarding data model consistency during analysis or of using a consistency database for storing consistency identifiers for comparison against consistency indicators of the data model. In particular, the comparisons within Matsumura (Fig. 1; Item 102, timing data; Abstract, L14-21; CL4, 29-43), as reference by the Examiner in section 8.1 of the pending office action, relate to comparison and synchronization of timing information stored within two memories; these are not related to data model consistency as in the present claims.

Beardslee discloses techniques and systems for debugging an electronic system having instrumentation circuitry. Specifically, Beardslee discloses debugging *fabricated* hardware designs at a Hardware Description Language (HDL) level. That is, the design has already been manufactured. Although Beardslee discloses performing license checks, version checks and consistency checks of the design instrumentation circuitry (DIC) and the design instrument database, Beardslee does not disclose creating a consistency database that contains consistency indicators for each block of interest in a data model. Beardslee does not relate to solving issues of a data model being modified between analyses, particularly since the device under test of Beardsley has been fabricated.

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Duffield discloses a system for processing a television signal including a data component. Specifically, Duffield discloses decoding time information from the video signal and comparing it to the time information maintained in the system to determine a time difference. If this time difference is in a predetermined range, it indicates that the time information from the television signal is invalid. Applicants can find no motivation to combine television signal decoding with and E-CAD tool to determining whether a model of a circuit design under analysis has been modified.

Tanaka discloses a method for centralizing the steps of designing a complex object. Specifically, Tanaka discloses a method of displaying steps of a process in a color that indicates whether the steps are executable or non-executable. See Tanaka Abstract. Tanaka makes no disclosure of a consistency database.

When applying 35 U.S.C. §103, the following tenets of patent law must be adhered to:

(A) The claimed invention must be considered as a whole;

(B) The references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination;

(C) The references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention; and

(D) Reasonable expectation of success is the standard with which obviousness is determined. MPEP §2141.01, Hodosh v. Block Drug Co., Inc., 786 F.2d 1136, 1134 n.5, 229 USPQ 182, 187 n.5 (Fed. Cir. 1986).

In addition, it is respectfully noted that to substantiate a *prima facie* case of obviousness, the initial burden rests with the Examiner who must fulfill three requirements. More specifically:

> **First**, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the references or to combine reference teachings.

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   <u>Second</u>, there must be a reasonable expectation of success.

   <u>Finally</u>, the prior art reference (or references when combined) must teach
or suggest all the claim limitations. The *teaching or suggestion* to make
the claimed combination and the ***reasonable expectation of success*** must
***both be found in the prior art***, and ***not based on applicant's disclosure***.
(emphasis and formatting added) MPEP § 2143, *In re vaeck*, 947 F.2d 488,
20 USPQ2d 1438 (Fed. Cir. 1991)

   We contend that the combination of Matsumura, Beardslee, Duffield and
Tanaka is neither desirable, nor obvious, and that the Examiner has mistakenly used
the benefit of impermissible hindsight in making an attempt to piecemeal-combine
Matsumura with vague, non-enabled and non-equivalent ideas in Beardslee, Duffield
and Tanaka, in an attempt to render Applicants' claims. This is impermissible under
35 U.S.C. §103. See, Ruiz v. A.B. Chance Co., 69 USPQ2d 1686 (CA FC 2004).

   The references used by the Examiner <u>must be considered in their entirety</u>. The
Examiner cannot piecemeal combine references in order to render Applicants'
invention. The Court has held that "...every element of a claimed invention may
often be found in the prior art. However, identification in the prior art of each
individual part claimed is insufficient to defeat patentability of the whole claimed
invention" *In re Rouffet*, 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1457 (Fed. Cir
1988).

   Further, it would not be obvious to combine a method for producing a test
pattern for use in an LSI tester (Matsumura) with a method for debugging fabricated
hardware designs (Beardslee), a system for processing a television signal (Duffield)
and a method for centralizing the steps of designing a complex object (Tanaka) when
trying to solve the problem of ensuring consistency of a data model being analyzed by
two or more sub-programs of an E-CAD tool (the '769 Application) since the
combination of test patterns, hardware debugger, television signal processing and
centralizing steps of design would not produce a useful result.

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Further, even when combined, Matsumura, Beardslee, Duffield and Tanaka do not render the '769 Application obvious.

Claim 1 recites a method for establishing consistency, with respect to a data model, between sub-modules within an E-CAD tool, including the steps of:

   a) creating a consistency database including at least one consistency indicator for each block of interest in the data model;

   b) executing one of the sub-modules to perform an analysis of a current version of the data model;

   c) comparing at least one data field value corresponding to said consistency indicator, for each block of interest, in source files in the current version of the data model being analyzed, against a corresponding said consistency indicator in the consistency database; and

   d) issuing a warning indicating a possible discrepancy between data in the current version of the data model and corresponding said data in a previous said version of the data model in the consistency database, in response to detecting a difference between said at least one data field value in the current version of the data model being analyzed and the corresponding said consistency indicator in the consistency database.

Step a) of claim 1 recites creating a consistency database including at least one consistency indicator for each block of interest in the data model. As taught by paragraphs [0011-14] of the '769 Application, the consistency database stores consistency indicators that specify a creation and/or last modification time of each block of interest within the data model. Neither Matsumura, Beardslee, Duffield nor Tanaka teach or suggest creating a consistency database including at least one consistency indicator for each block of interest in the data model, as required by step a). As noted by the Examiner in section 8 of the pending office action, neither Matsumura nor Beardslee disclose issuing a warning indicating possible discrepancies between data in the current version of the data model. The Examiner implies that it would be obvious to combine Duffield with Matsumura and Beardslee "because that would prevent modification of a second data when the difference in data is outside a range." See section 8 of the pending office action. With all due respect, Applicants

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can find no motivation for combining television signal processing with Matsumura and Beardslee. Clearly, the Examiner includes Duffield with regard to step d) of claim 1, and does not consider either the '769 Application in its entirety, nor Duffield in its entirety, and therefore fails to comply with at least tenants (A) and (B) of patent law, listed above. With regard Tanaka, the Examiner asserts that in column 12, lines 43-53, Tanaka teaches data in the current version of the data model and corresponding data in a previous version of the data model, and detecting the at least one data field value in the current version of the data model being analyzed. Respectfully we disagree. In our understanding, the section of Tanaka referenced by the Examiner in section 8 of the pending office action relates to a version control system that saves the design data generated by the CAD tools and the design environment within a design database (D/B 205). The version control system of Tanaka provides only a way of identifying saved versions of the design data and design environment (e.g., the provided serial number). Tanaka makes no disclosure of comparing at least one data field value corresponding to said consistency indicator, for each block of interest, in source files in the current version of the data model being analyzed, against a corresponding said consistency indicator in the consistency database, as required by step c) of claim 1. Again, the Examiner does not appear to consider either the '769 Application in its entirety, nor Tanaka in its entirety, and therefore fails to comply with at least tenants (A) and (B) of patent law, listed above. In fact, the reason provided by the Examiner for combining Tanaka with Matsumura, Beardslee and Duffield, "that would enable sharing of data relating to design between devices realizing cooperative work by a plurality of designers," creates the very problem solved by the '769 Application.

For at least these reasons Matsumura, Beardslee, Duffield and Tanaka cannot render claim 1 obvious. Reconsideration of claim 1 is respectfully requested.

Claim 4 depends from claim 1 and benefits from like argument. Reconsideration of claim 4 is respectfully requested.

9. Claims 7 and 10-12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Matsumura in view of Duffield and further in view of Tanaka.

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Claim 7 recites a system for establishing consistency, with respect to a data model, between sub-modules within an E-CAD tool, comprising:

a) a processor;

b) a consistency database, accessible by the processor, for storing consistency information for each block of interest in the data model;

c) a comparison module, capable of accessing the consistency database and executable via said processor, for comparing at least one data field value, corresponding to said consistency information, against corresponding said consistency information; and

d) an interface module, responsive to detection of a difference between said data field value in a current version of the data model being analyzed and a corresponding said consistency information in a consistency database, for issuing a warning indicating a possible discrepancy between data in the current version of the data model and corresponding said data in a previous said version of the data model.

The reasons noted above regarding non-obviousness of combining Matsumura, Duffield and Tanaka are applicable with regard to the rejection of claim 7. Further, as argued above, neither Matsumura, Duffield nor Tanaka disclose or suggest creating a consistency database including at least one consistency indicator for each block of interest in the data model, as required to render element b) of claim 7 obvious. The timing data within the timing file $10_2$, FIG. 1, of Matsumura is created from the dump file 15 resulting from performing a logic simulation in the design stage of the LSI device. This does not represent a consistency database of consistency information as required by element b) of claim 7. Element c) of claim 7 requires a comparison module for comparing at least one data field value against corresponding consistency information within the consistency database. Contrary to the Examiner's assertion, Matsumura does not disclose a comparison module for comparing consistency information within the consistency database against corresponding consistency information within a data field of a current version of the data model being analyzed.

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For at least these reasons, Matsumura, Duffield and Tanaka cannot render claim 7 obvious. Reconsideration of claim 7 is respectfully requested.

Claims 10 -12 depend from claim 7 and benefit from like argument. However, these claims have additional features that patentable distinguish over Matsumura, Duffield and Tanaka. For example, claim 10 recites that the comparison module is functionally integrated into each of a plurality of the sub-modules. Matsumura, Duffield and Tanaka make no disclosure of a comparison module integrated into each of the plurality of sub-modules of an E-CAD tool. Claim 11 recites that a plurality of the sub-modules are simultaneously operational. Matsumura make no disclosure of sub-modules of an E-CAD tool being simultaneously operational. Claim 12 recites that said comparison module is functionally independent of each of the sub-modules. Since Matsumura make no disclosure of a comparison module for comparing consistency information, Matsumura cannot disclose of the comparison module being independent of sub-modules of an E-CAD tool.

For at least these reason, Matsumura, Duffield and Tanaka cannot render claims 10-12 obvious. Reconsideration of claims 10-12 is respectfully requested.

**10.** Claims 2,5,13,14,16-19 stand rejected under 35 U.S. C. 103(a) as being unpatentable over Matsumura, in view of Beardslee, Duffield and Tanaka, and further in view of U.S. Patent 6,377,912 granted to Sample et al. (hereinafter, "Sample") and U.S. Patent 6,009,251 granted to Ho et al. (hereinafter, "Ho").

Sample discloses an emulation system with time multiplexed interconnect. Specifically, Sample discloses a reconfigurable logic system with a plurality of reprogrammable logic devices and a plurality of reprogrammable interconnect devices. Sample utilizes a timestamp to order frames stored in random order within a block of memory located on a logic board. Sample is not related to sub-modules of an E-CAD tool or to evaluating consistency information relating to blocks of interest within a data model.

Ho discloses a method and system for layout verification of an integrated circuit design using reusable subdesigns. Specifically, Ho utilizes a hierarchical tree structure to represent an integrated circuit design. The integrated circuit design is

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typically stored as a netlist within a number of interrelated files within subdirectories of a computer disk unit. See Ho col. 8 lines 40-42. A layout verification process 255 checks for design rule violations of the layout and layout versus schematic errors. On subsequent layout verification of a netlist, the layout verification process 255 reuses any unchanged subcell design that was previously verified, thereby avoiding otherwise redundant design rule checking and layout versus schematic checking. Ho discloses that "it is appreciated that the time and date of creation of the subcell design are also part of the file name. In alternative embodiment, the time and date of the last modification is also a part of the name. The tree hierarchical level is created based on time creation of one of the source file." See Ho col. 13, lines 22-25.

The Examiner again attempts to piecemeal-combine Sample and Ho with Matsumura, Beardslee, Duffield and Tanaka to include the timestamp feature of Sample and the file creation time of Ho. See section 10.1 of the pending office action. The '769 Application, Sample and Ho must be considered as a whole and suggest the obviousness of making the combination with Matsumura, Beardslee, Duffield and Tanaka. Respectfully, the Examiner again uses the benefit of impermissible hindsight in making an attempt to piecemeal-combine Matsumura with vague, non-enabled and non-equivalent ideas in Beardslee, Duffield and Tanaka, Sample and Ho in an attempt to render Applicants' claims. This is impermissible under 35 U.S.C. §103. See, Ruiz v. A.B. Chance Co., 69 USPQ2d 1686 (CA FC 2004).

10.1    Claim 2 depends from claim 1 and benefits from the arguments presented above regarding claim 1. Claim 2 recites that the consistency indicator comprises timestamp information indicating a time of creation of one of the source files. Although Sample discloses a timestamp and Ho discloses a file creation time, Sample and Ho do not overcome the shortfall of Matsumura, Beardslee, Duffield and Tanaka in rendering claim 1 obvious. For example, Sample and Ho, even when combined, do not teach creating a consistency database including at least one consistency indicator for each block of interest in the data model, or teach executing one of the sub-modules to perform an analysis of a current version of the data model, or teach comparing at least one data field value corresponding to said consistency indicator, for each block of interest, in source files in the current version of the data

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model being analyzed, <u>against a corresponding said consistency indicator in the</u> <u>consistency database</u>. More specifically, neither Matsumura, Beardslee, Duffield, Tanaka, Sample nor Ho disclose use of the time stamp and file creation time as a consistency indicator for determining consistency of a data model being analyzed by sub-programs of an E-CAD tool. Reconsideration of claim 2 is respectfully requested.

    **10.2**    Claim 13 recites a system for establishing consistency, with respect to a data model, between sub-modules within an E-CAD tool, including:

    a)   means for creating a consistency database including at least one consistency indicator for each block of interest in the data model;

    b)   means for executing one of the sub-modules to perform an analysis of a current version of the data model;

    c)   means for comparing a data field value corresponding to said consistency indicator, for each block of interest, in source files in the current version of the data model being analyzed, against a corresponding said consistency indicator in the consistency database;

    d)   wherein the consistency indicator comprises timestamp information indicating at least one of a time of creation and a time of modification of one of the source files; and

    e)   means for issuing a warning indicating a possible discrepancy between data in the version of the data model being analyzed and corresponding said data in a previous said version of the data model, in response to detecting a difference between said data field value in the current version of the data model being analyzed and the corresponding said consistency indicator.

Matsumura does not disclose or suggest establishing consistency with respect to a data model between sub-modules within an E-CAD tool. As argued above, the dump file of Matsumura is not equivalent to a consistency database, and Matsumura makes no disclosure of including at least one consistency indicator for each block of interest in the data model. The timing data within the timing file $10_2$, FIG. 1, of

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Matsumura is created from the dump file 15 resulting from performing a logic simulation in the design stage of the LSI device. This does not represent a consistency database of consistency information as required by element a). Element c) requires means for comparing a data field value corresponding to said consistency indicator, for each block of interest, in source files in the current version of the data model being analyzed, against a corresponding said consistency indicator in the consistency database. Contrary to the Examiner's assertion, Matsumura does not disclose a comparison module for comparing consistency information within the consistency database against corresponding consistency information within a data field of a current version of the data model being analyzed.

Beardslee does not make up for the shortfall of Matsumura in rendering elements a) and c) of claim 13 obvious. Further, Beardslee does not disclose or suggest means for comparing a data field value corresponding to the consistency indicator for each block of interest within the data model, as asserted by the Examiner.

Sample does not overcome the shortfall of Matsumura in rendering elements a) and c) of claim 13 obvious. Although Sample discloses timestamp values, these values are saved to a memory within a control board 600 each time a frame is saved on logic boards 200. The timestamp values of Sample do not relate to consistency indicators and a consistency database. Ho also does not overcome the shortfall of Matsumura in rendering elements a) and c) of claim 13 obvious. Although Ho discloses that a filename may include a time and date of creation or modification, Ho makes no disclosure of utilizing this time and date is association with a consistency database.

Duffield does not overcome the shortfall of Matsumura in rendering elements a) and c) of claim 13 obvious. As noted above, the reasons for combining Duffield with Matsumura are not obvious, since Duffield relates to processing of a television signal. Duffield compares a time determined from the video signal to a time maintained within the system to determine if the time information is valid. The time of Duffield is not related to consistency of blocks of interest in a data model.

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For at least these reasons, Matsumura, Beardslee, Duffield, Tanaka, Sample and Ho cannot render claim 13 obvious. Reconsideration of claim 13 is respectfully requested.

**10.3** Claim 14 depends from claim 13 and benefits from like argument. Reconsideration of claim 14 is respectfully requested.

Claim 16 depends from claim 13 and benefits from like argument. Claim 16 also has additional features that patentable distinguish over Matsumura, Beardslee, Duffield, Tanaka, Sample and Ho. For example, claim 16 recites that the means for issuing a warning is functionally integrated into each of a plurality of the sub-modules. Neither Matsumura, Beardslee, Duffield, Tanaka, Sample nor Ho disclose or suggest functionally integrating the means for issuing a warning into each of a plurality of sub-modules. The Examiner asserts, in section 10.3, that Duffield teaches that the means for issuing a warning is functionally integrated into each of a plurality of sub-modules. Respectfully we disagree, since Duffield does not even disclose or suggest an E-CAD tool, let alone sub-modules thereof. Reconsideration of claim 16 is respectfully requested.

Claim 17 depends from claim 13 and benefits from like argument. Claim 17 also has other features that patentably distinguish over Matsumura, Beardslee, Duffield, Tanaka, Sample and Ho. For example, claim 17 recites that a plurality of the sub-modules are simultaneously operational. The Examiner asserts, in section 10.3 of the pending office action, that Matsumura teaches that a plurality of sub-modules are simultaneously operational. Respectfully we disagree. Although, Matsumura discloses evaluating a test pattern produced based upon the CAD data derived in the design stage of the LSI device, Matsumura does not disclose or suggest simultaneous sub-module operation anywhere. It seems again that the Examiner uses impermissible hindsight when interpreting Matsumura. Reconsideration of claim 17 is respectfully requested.

**10.4** Claim 5 stands rejected based on the same reasoning as claim 13. Arguments in response to the rejection of claim 13 are hereby incorporated in

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response to the rejection of claim 5. Reconsideration of claim 5 is respectfully requested.

    **10.5**    Claim 18-19 are rejected based on the same reasoning as claims 13 and 14. Arguments in response to the rejection of claims 13 and 14 are hereby incorporated in response to the rejection of claims 18 and 19. Reconsideration of claims 18 and 19 is respectfully requested.

    **11.**    Claim 8 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumura in view of Duffield and Tanaka and further in view of Sample and Ho. Respectfully we disagree.

    **11.1**    Claim 8 depends from claim 7. Arguments in response to the rejection of claim 7 are incorporated herein in response to the rejection of claim 8. Reconsideration of claim 8 is respectfully requested.

We thank the Examiner for indication of allowable subject matter in claims 3, 6, 9, 15, and 20.

In view of the above amendments and arguments, all of pending claims 1- 20 are believed allowable. Matsumura, Beardslee, Duffield, Tanaka, Sample, and Ho alone or in combination do not establish *prima facie* obvious over any pending claim. We respectfully solicit a Notice of Allowance for all pending claims.

The Examiner is encouraged to telephone Applicant's attorney, Curtis A. Vock, at (720) 931-3011 to discuss the amendments presented herein, or any outstanding issues regarding the '769 Application. We respectfully request the Examiner's call prior to the mailing of any further Office Communication.

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No fees are believed due; however, if any fee is deemed necessary in connection with this Amendment and Response, the Commissioner is authorized to charge such fee to Deposit Account No. 08-2025.

Respectfully submitted,

By:  ⟨signature⟩
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